REMARKS

The Official Action dated November 29, 2005 has been received and its contents carefully noted. In view of the following remarks, it is respectfully requested that the rejection of record be reconsidered and withdrawn by the Examiner, and that claims 1 and 3-10 be allowed. In this regard, claims 1 and 3-10 are presently pending in the instant application.

Initially, it is noted from the previous Office Action that claims 2-4 were objected to as dependent upon a rejected base claim but would have been allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. In this regard the subject matter of previous dependent claim 2 was included in independent claim 1 and consequently it was believed that independent claim 1 was now in proper condition for allowance. However, in the present Office Action, each of claims 1 and 3-5 have been rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent Publication 2002/0019898 to Hayashi et al. which is the same reference set forth in the previous Office Action. Further, there can be found no detailed explanation as to why the subject matter of previous claim 2 is now not considered to be allowable. However, Applicant does acknowledge with appreciation that the present Office Action has been made non-final. For the reasons discussed in detail hereinbelow, it is respectfully submitted that independent claim 1 as well as those claims which depend therefrom along with claims 6-10 clearly distinguish over the prior art of record and are in proper condition for allowance.

Applicant wishes to acknowledge the Examiner's indication that claims 6-10 are allowable over the prior art of record.

With reference now to page 2 of the Office Action, claims 1 and 3-5 have been rejected under 35 U.S.C. §102(b) as being anticipated by Hayashi et al. This rejection is

respectfully traversed in that the publication to Hayashi et al. neither discloses nor suggests that which is presently set forth by Applicant's claimed invention.

As presently recited in independent claim 1, Applicant's claimed invention is directed to a system LSI comprising a group of external terminals to which a plurality of external devices can be connected, the process or carrying out computation and control on the basis of programs, a bus interface specifying an external device which is to be an object of access from among the plurality of external devices on the basis of a control signal outputted from the processor, and outputting access time data instructing an access time to the external device and a request signal requesting access to the external device, a register storing the access time data output from the bus interface, an input terminal to which is inputted, from an exterior, a wait signal which designates extension of the access time to the external device and an external bus controller which, in accordance with the access time data stored in the register and the request signal outputted from the bus interface, accesses the external device by way of the group of external terminals, and extends the access time to the external device in accordance with the wait signal inputted to the input terminal, wherein the external bus controller extends the access time to the external device in units of the access time which the access time of data instructs. Particularly, the present invention includes an input terminal and an external bus controller wherein the input terminal receives a wait signal (MWAIT in Fig. 1) which designates extensions of an access time to an external device and the external bus controller extends the access time to an external device. In doing so, the system LSI set forth in accordance with Applicant's claimed invention can be tested in an operational mode of a clock speed higher than that of ordinary operational conditions. Clearly, these features are neither disclosed in nor suggested by the teachings of Hayashi et al.

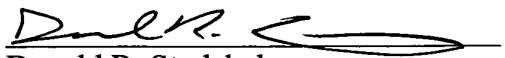
With respect to the teachings of Hayashi et al., the wait signal disclosed therein and as particularly described in the specification of Hayashi et al., is for inserting a wait state into a

cycle making access to a low-speed memory address area. That is, this teaching is not limited to extending access to a high-speed memory address area. Accordingly, this is merely a signal that is inserted between switching from a high-speed memory clock to a low-speed clock and thus neither discloses nor remotely suggests that which is presently set forth by Applicant's claimed invention. Furthermore, it is noted that Hayashi et al. fails to include an input terminal in the LSI system for inputting a wait signal and thus any such signal included in Hayashi et al. would merely have to be generated internally. Consequently, it is respectfully submitted that Applicant's claimed invention, which recites limitations that are clearly neither disclosed in nor suggested by Hayashi et al., distinguishes over the teachings thereof and are in proper condition for allowance.

Therefore, it is respectfully requested that the rejection of record be reconsidered and withdrawn by the Examiner, that claims 6-10, again, be indicated as being allowable, that claims 1 and 3-5 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,



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